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EXAMINER	
HUISMAN, DAVID J	

ART UNIT	PAPER NUMBER
2183	5

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/702,405	Applicant(s) HOYLE ET AL.
	Examiner David J. Huisman	Art Unit 2183

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *31 October 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-14 have been examined.

Papers Submitted

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: #3. Declaration as received on 2/13/2001 and #4. IDS as received on 10/31/2001.

Specification

3. The abstract of the disclosure is objected to because of the following minor informalities: Please remove reference labels 600, 602, and 702. Also, "Figure 6A-6L" should be removed from the end of the abstract.

4. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

5. The disclosure is objected to because of the following informalities: Please remove all attorney docket number references and provide application or patent numbers along with titles when mentioning other related applications. Insert a comma after ".D1" on page 14, line 20. Furthermore, on page 19, lines 12-13, the examiner is unclear on what BK0 and BK1 are (a further explanation should be provided). On page 27, line 3, replace "instructions" with

--instruction--. On page 31, line 21, replace "700ca" with --700c--. Finally, on page 34, the paragraph beginning on lime 12 doesn't seem to accurately describe Fig.8. A lot of the number references are incorrect. This should be rewritten so that it better described Fig.8.

Appropriate correction is required.

Drawings

6. The drawings are objected to because of the following minor informalities: In Fig.1, component 82 should be labeled. Also, it is not clear from the specification and the drawings (Fig.5A, for instance) how the s-bit selects a functional unit as described on page 27, lines 8-9. In Fig.7B, it is not clear what the first two inputs of each MUX 730(3)-730(0) are labeled as. Also, in Fig.7C, it is not clear what the first inputs of MUX 740(3) and 740(1) are labeled as. Also, it is not clear why each MUX supposedly has 3 inputs (A, B, and C), yet each of the MUXs contains more than 3 inputs. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: In Fig.1, labels 43, 82, 90, and 100 have not been found by the examiner within the specification. In Fig.2, labels 12a,b, 14a,b, 16a,b, 210, 213, 214, 220, 221, 102, and 250 have not been found by the examiner within the specification. In Fig.6A, label 610(0) has not been found by the examiner within the specification. In Fig.7B, label 734 has not been found by the examiner within the specification. In Fig.7C, label 744 has not been found by the examiner within the specification. In Fig.8, labels 1001, 1010a, 1010b, 1020a, and 1020b have not been found by the examiner within the

specification. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application.

8. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "10" and "40" in Fig.9 have both been used to designate the cell-phone's processor. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The objection to the drawings will not be held in abeyance.

Claim Objections

9. It is recommended that the applicant use subscripts throughout all of the claims so that N1, N2, and N3 read as N_1, N_2, and N_3, respectively. This would make the claims easier to read and eliminate any possible confusion that would arise from reading N1-1, as shown in claim 3.

10. Claim 3 is objected to because of the following informalities: Remove the word "a" before "N1-1". Appropriate correction is required.

11. Claim 4 is objected to because of the following informalities: On page 39, line 10, replace "the" with --to--. Appropriate correction is required.

12. Claim 5 is objected to because of the following informalities: On page 39, line 17, replace "the" with --to--. Appropriate correction is required.

13. Claim 7 is objected to because of the following informalities: On page 40, line 2, remove the second occurrence of "operable to". Appropriate correction is required.

14. Claim 8 is objected to because of the following informalities: On page 40, line 10, remove the second occurrence of "operable to". On page 40, line 13, insert the word --of-- after "significant one". Appropriate correction is required.

15. Claim 12 is objected to because of the following informalities: On page 41, line 8, insert --and-- after "microprocessor". On page 41, line 9, replace "instruction" with --instructions--. Appropriate correction is required.

16. Claim 13 is objected to because of the following informalities: On page 41, line 27, insert --of-- after "second type". Appropriate correction is required.

Claim Rejections - 35 USC § 112

17. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

18. Claim 6 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 6 contains what the examiner believes to be an informality, which results in the operation of claim 6 not being an operation described in the specification. The examiner believes that "most" on page 39, line 25, should be replaced with --least-- so that the operation corresponds to a swap operation (this is how the claim will be interpreted for examination purposes).

19. Claim 7 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 7 contains what the examiner believes to be an informality, which results in the operation of claim 7 not being an operation described in the specification. The examiner believes that "second" on page 40, line 5, should be replaced with --first-- so that the operation corresponds to a byte pack operation (this is how the claim will be interpreted for examination purposes).

20. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

21. Claim 4 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted element is the placing of the selected first N_1-1 fields from a most significant portion of the second operand into the destination operand. A merge operation (as claimed) cannot be performed if the selected fields from the second operand are not written to the destination.

22. Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential elements, such omission amounting to a gap between the elements. See MPEP § 2172.01. The omitted element is the placing of the selected second N_1-1 fields from a least significant portion of the second operand into the destination operand. A merge operation (as

claimed) cannot be performed if the selected fields from the second operand are not written to the destination.

23. Claim 11 recites the limitation "the CPU" in lines 3-5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

24. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

25. Claims 1, 3, 6-10, and 12-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Intel, IA-64 Application Developer's Architecture Guide, May 1999 (herein referred to as Intel) in view of Hennessy and Patterson, Computer Architecture - A Quantitative Approach, 2nd Edition, 1996 (herein referred to as Hennessy).

26. Referring to claim 1, Intel has taught a digital system comprising a microprocessor, wherein the microprocessor comprises:

a) program fetch circuitry. See page 6-2, section 6.1.1 and note that instructions are fetched by the processor. It is inherent that some circuitry must exist in order to allow for the fetching of instructions.

b) instruction decode circuitry. See page 6-2, section 6.1.1 and note that instructions are decoded by the processor. It is inherent that decode circuitry must exist in order to allow for the decoding of instructions.

c) at least a first functional unit connected to receive control signals from the instruction decode circuitry. See page 6-2, section 6.1.1 and note that instructions are executed by the processor. It is inherent that a functional unit would exist in order to perform such executions.

d) the functional unit comprising byte intermingling circuitry connected to receive a first source operand and a second source operand and having outputs connected to provide a destination operand in response to the control signals, wherein the byte intermingling circuitry is operable to treat the first and second operands each as a number N_1 of ordered fields, such that the destination operand consists of a number N_2 of fields selected from the N_1 fields of the first source operand intermingled with a number N_3 of fields selected from the N_1 fields of the second source operand. For instance, see page 7-117 and note that source operands r2 and r3 each contain N_1 fields wherein a number N_2 of r2's fields and a number N_3 of r3's fields are written to a destination.

e) the first functional unit is operable to provide the destination operand intermingled in accordance to each of a set of byte intermingling instructions. See page 7-117 and note that r1 is the destination for the intermingled bytes of sources r2 and r3.

f) Although Intel has suggested the use of a pipeline (see page 11-13, section 11.3.4), Intel has not explicitly taught a plurality of pipeline phases, wherein the fetch circuitry performs a first portion of the plurality of pipeline phases, the decode circuitry performs a second portion of the plurality of pipeline phases and the functional unit performs a third portion of the plurality of pipeline phases, the third portion being execution phases. However, Hennessy has taught a plurality of pipeline phases, which includes a first fetch phase (IF), a second decode phase (ID), and a third execute phase (EX). See Figure 3.2 on page 132. As can be seen from the Figure's

description and from pages 125-126 of Hennessy, pipelining increases the amount of parallelism within a processor. More specifically, instructions can be executed in parallel as opposed to serially. This results in an increase in throughput since a new instruction can be started every cycle as opposed to starting only when the previous instruction ends. As a result, execution speed is increased. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a plurality of pipeline phases in Intel as taught by Hennessy.

27. Referring to claim 3, Intel in view of Hennessy has taught a digital system as described in claim 1. Intel has further taught that the byte intermingling circuitry is operable to provide a destination operand that consists of a N_1-1 fields selected from the second operand and one field selected from the first source operand. For instance, see the "mix4.r" instruction on page 7-117. Note that $N_1 = 2$ for both sources. It should be further noted that 1 field is selected from the first source (r2) and N_1-1 fields are selected from the second source (r3), where N_1-1 = 1.

28. Referring to claim 6, Intel in view of Hennessy has taught a digital system as described in claim 1. Intel has further taught that the byte intermingling circuitry is operable to provide the destination operand by placing a most significant set of the N_1 fields selected from the second operand in a least significant portion of the destination operand and by placing a least significant set of the N_1 fields selected from the second operand in a most significant portion of the destination, whereby a byte swap operation is performed. See page 7-131 and note the mux-reverse instruction (top right illustration in Figure 7-25). Note that the most significant set of the 4 fields (bytes 2 and 3) are placed in a least significant portion (bytes 1 and 0) of the destination.

Also note that the least significant set of the 4 fields (bytes 0 and 1) are placed in a most significant portion (bytes 3 and 2) of the destination.

29. Referring to claim 7, Intel in view of Hennessy has taught a digital system as described in claim 6. Intel has further taught that the byte intermingling circuitry is operable to provide the destination operand by placing a least significant set of the N_1 fields selected from the second operand in a least significant portion of the destination operand and by placing a least significant set of the N_1 fields selected from the first operand in a most significant portion of the destination, whereby a byte pack operation is performed. See the "mix4.r" instruction on page 7-117. Note that the least significant set of 1 field of both r2 and r3 are written to a most and least significant portion of the destination, respectively.

30. Referring to claim 8, Intel in view of Hennessy has taught a digital system as described in claim 6. Intel has further taught that the byte intermingling circuitry is operable to provide the destination operand by placing a least significant one of the N_1 fields selected from the second operand in a least significant portion of the destination operand and by placing a next to least significant one of the N_1 fields selected from the second operand in a most significant portion of the destination, whereby a byte unpack operation is performed. See the "unpack2.l" instruction on page 7-183.

31. Referring to claim 9, Intel in view of Hennessy has taught a digital system as described in claim 1. Intel has further taught a register file connected to the first functional unit for providing the first and second source operands and connected to the first functional unit to receive the destination operand. See pages 3-1 and 9-1 and note that the processor contains multiple types

of registers. The general purpose registers and floating-point registers would be those used as sources and destinations in the aforementioned operations.

32. Referring to claim 10, Intel in view of Hennessy has taught a digital system as described in claim 1. Intel has further taught each of the set of byte intermingling instructions has a field for identifying a predicate register. See page 9-2 and more specifically the "qp" field in section 9.3.1, which discusses the format of a basic IA-64 instruction.

33. Referring to claim 12, Intel has taught a method of operating a digital system having a microprocessor and a set of byte intermingling instructions, comprising the steps of:

a) fetching a first type of byte intermingling instruction for execution. See page 6-2, section 6.1.1 and note that instructions are fetched by the processor. Note that one of the instructions fetched can be one of the byte-intermingling instructions shown in chapter 7 (for instance, the first instruction fetched may the "mix2.l" instruction).

b) fetching a first source operand and a second operand selected by the first type of byte intermingling instruction. See page 7-116 and 7-117 and note that the first instruction requires two source operands, which have to be fetched.

c) treating the first and second source operands as a set of N_1 fields. See page 7-117 again and note that each source operand is divided into N_1 fields.

d) intermingling selected ones of the N_1 fields from the first operand and selected ones of the N_1 fields from the second operand in a first selected order in accordance with the first type of byte intermingling instruction to form a first type of intermingled fields. See page 7-117 again and note that this type of byte intermingling instruction results in the selection of ones of the N_1 fields from both the first and second source operands.

e) writing a destination operand with the first type of intermingled fields. See page 7-117 and note that the intermingled fields are written to a destination operand (in this case, register r1).

34. Referring to claim 13, Intel has taught a method as described in claim 12. Intel has further taught:

a) fetching a second type of byte intermingling instruction for execution. See page 6-2, section 6.1.1 and note that instructions are fetched by the processor. It should be realized that a second type of byte intermingling instruction could be fetched (for instance, the second instruction might be "mix2.r").

b) fetching a first source operand and a second operand selected by the second type of byte intermingling instruction. See page 7-116 and 7-117 and note that this instruction requires two source operands, which have to be fetched.

c) treating the first and second source operands as a set of N_1 fields. See page 7-117 again and note that each source operand is divided into N_1 fields.

d) intermingling selected ones of the N_1 fields from the first operand and selected ones of the N_1 fields from the second operand in a second selected order in accordance with the second type of byte intermingling instruction to form a second type of intermingled fields. See page 7-117 again and note that this type of byte intermingling instruction results in the selection of ones of the N_1 fields from both the first and second source operands.

e) writing a destination operand with the second type of intermingled fields. See page 7-117 and note that the intermingled fields are written to a destination operand (in this case, register r1).

35. Claims 1-9 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Philips Electronics, TM 1000 Preliminary Data Book, 1997 (herein referred to as Philips) in view of Hennessy, as applied above.

36. Referring to claim 1, Philips has taught a digital system comprising a microprocessor, wherein the microprocessor comprises:

a) program fetch circuitry. It is inherent that instructions are fetched by the processor. Therefore, some circuitry must exist in order to allow for the fetching of instructions. If instructions were not fetched then the processor would not be able to execute a program.

b) instruction decode circuitry. It is inherent that instructions are decoded by the processor. Therefore, decode circuitry must exist in order to allow for the decoding of instructions. Instruction decoding is the process of determining what operation is to be performed by the instruction and preparing the circuits in the computer to execute the instruction.

c) at least a first functional unit connected to receive control signals from the instruction decode circuitry. It is inherent that instructions are executed by the processor. Therefore, a functional unit would exist in order to perform such executions.

d) the functional unit comprising byte intermingling circuitry connected to receive a first source operand and a second source operand and having outputs connected to provide a destination operand in response to the control signals, wherein the byte intermingling circuitry is operable to treat the first and second operands each as a number N_1 of ordered fields, such that the destination operand consists of a number N_2 of fields selected from the N_1 fields of the first source operand intermingled with a number N_3 of fields selected from the N_1 fields of the second source operand. For instance, see page A-60 and note that source operands rsrc1 and rsrc2 each

contain N_1 fields wherein a number N_2 of rsrc2's fields and a number N_3 of rsrc3's fields are written to a destination.

e) the first functional unit is operable to provide the destination operand intermingled in accordance to each of a set of byte intermingling instructions. See page A-60 and note that rdest is the destination for the intermingled bytes of sources rsrc1 and rsrc2.

f) Philips has not explicitly taught a plurality of pipeline phases, wherein the fetch circuitry performs a first portion of the plurality of pipeline phases, the decode circuitry performs a second portion of the plurality of pipeline phases and the functional unit performs a third portion of the plurality of pipeline phases, the third portion being execution phases. However, Hennessy has taught a plurality of pipeline phases, which includes a first fetch phase (IF), a second decode phase (ID), and a third execute phase (EX). See Figure 3.2 on page 132. As can be seen from the Figure's description and from pages 125-126 of Hennessy, pipelining increases the amount of parallelism within a processor. More specifically, instructions can be executed in parallel as opposed to serially. This results in an increase in throughput since a new instruction can be started every cycle as opposed to starting only when the previous instruction ends. As a result, execution speed is increased. Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement a plurality of pipeline phases in Philips as taught by Hennessy.

37. Referring to claim 2, Philips in view of Hennessy has taught a digital system as described in claim 1. Philips has further taught that the byte intermingling circuitry is operable to receive the first source operand and second operand and to provide the destination operand during a single pipeline execution phase. See page A-60 again and note that the latency of this particular

byte-intermingling instruction is a single cycle. Also, in order for the intermingling to occur, the intermingling circuitry must receive the first and second operands (as shown in A-60).

38. Referring to claim 3, Philips in view of Hennessy has taught a digital system as described in claim 1. Philips has further taught that the byte intermingling circuitry is operable to provide a destination operand that consists of a N_1-1 fields selected from the second operand and one field selected from the first source operand. For instance, see the "funshift3" instruction on page A-62. Note that $N_1 = 4$ for both sources. It should be further noted that one field is selected from the first source (rsrc1) and N_1-1 fields are selected from the second source (rsrc2), where N_1-1 = 3.

39. Referring to claim 4, Philips in view of Hennessy has taught a digital system as described in claim 3. Philips has further taught that the byte intermingling circuitry is operable to select a first N_1-1 fields from a most significant portion of the second operand and to select a first field from a least significant portion of the first operand, such that the first field from the first operand is placed in a most significant portion of the destination operand, whereby a shift right and byte merge operation is performed. See the "funshift3" instruction on page A-62.

40. Referring to claim 5, Philips in view of Hennessy has taught a digital system as described in claim 4. Philips has further taught that the byte intermingling circuitry is operable to select a second N_1-1 fields from a least significant portion of the second operand and to select a second field from a most significant portion of the first operand, such that the second field from the first operand is placed in a least significant portion of the destination operand, whereby a shift left and byte merge operation is performed. See the "funshift1" instruction on page A-60. It should be noted that a second field is selected from a most significant portion of the first operand (in this

case, the first operand is rsrc2) and placed into a least significant portion of the destination operand. In addition, N_1-1 fields are selected from the least significant portion of the second source (in this case, the second operand is rsrc1), where N_1-1 = 3.

41. Referring to claim 6, Philips in view of Hennessy has taught a digital system as described in claim 1. Philips has further taught that the byte intermingling circuitry is operable to provide the destination operand by placing a most significant set of the N_1 fields selected from the second operand in a least significant portion of the destination operand and by placing a least significant set of the N_1 fields selected from the second operand in a most significant portion of the destination, whereby a byte swap operation is performed. See Figure C-2 on page C-2. Note that the most significant set of the 4 fields (bytes 2 and 3) are placed in a least significant portion (bytes 1 and 0) of the destination. Also note that the least significant set of the 4 fields (bytes 0 and 1) are placed in a most significant portion (bytes 3 and 2) of the destination.

42. Referring to claim 7, Philips in view of Hennessy has taught a digital system as described in claim 6. Philips has further taught that the byte intermingling circuitry is operable to provide the destination operand by placing a least significant set of the N_1 fields selected from the second operand in a least significant portion of the destination operand and by placing a least significant set of the N_1 fields selected from the first operand in a most significant portion of the destination, whereby a byte pack operation is performed. See the "pack16lsb" instruction on page A-136. Note that the least significant set of 1 field of both rsrc1 and rsrc2 are written to a most and least significant portion of the destination, respectively.

43. Referring to claim 8, Philips in view of Hennessy has taught a digital system as described in claim 6. Philips has further taught that the byte intermingling circuitry is operable to provide

the destination operand by placing a least significant one of the N_1 fields selected from the second operand in a least significant portion of the destination operand and by placing a next to least significant one of the N_1 fields selected from the second operand in a most significant portion of the destination, whereby a byte unpack operation is performed. See the "mergelsb" instruction on page A-133.

44. Referring to claim 9, Philips in view of Hennessy has taught a digital system as described in claim 1. Philips has further taught a register file connected to the first functional unit for providing the first and second source operands and connected to the first functional unit to receive the destination operand. See page 3-1 and note that the processor contains 128 general-purpose registers. The general-purpose registers would be those used as sources and destinations in the aforementioned operations.

45. Referring to claim 12, Philips has taught a method of operating a digital system having a microprocessor and a set of byte intermingling instructions, comprising the steps of:

a) fetching a first type of byte intermingling instruction for execution. It is inherent that instructions are fetched by the processor. Therefore, some circuitry must exist in order to allow for the fetching of instructions. If instructions were not fetched then the processor would not be able to execute a program. It should also be noted that any one of the instruction fetched could be one of the instructions shown in Appendix A of Philips, which includes the byte-intermingling instructions.

b) fetching a first source operand and a second operand selected by the first type of byte intermingling instruction. See page A-60, for instance, and note that these instructions require two source operands, which have to be fetched.

c) treating the first and second source operands as a set of N_1 fields. See page A-60 again and note that each source operand is divided into N_1 fields (in this case, $N_1 = 4$).

d) intermingling selected ones of the N_1 fields from the first operand and selected ones of the N_1 fields from the second operand in a first selected order in accordance with the first type of byte intermingling instruction to form a first type of intermingled fields. See page A-60 again and note that this type of byte intermingling instruction results in selecting ones of the N_1 fields from both the first and second source operands.

e) writing a destination operand with the first type of intermingled fields. See page A-60 and note that the intermingled fields are written to a destination operand (in this case, register rdest).

46. Referring to claim 13, Philips has taught a method as described in claim 12. Philips has further taught:

a) fetching a second type of byte intermingling instruction for execution. As established in the rejection of claim 12, it is inherent that instructions are fetched by the processor. It should be realized that a second type of byte intermingling instruction could be fetched (such as the one shown on page A-61).

b) fetching a first source operand and a second operand selected by the second type of byte intermingling instruction. See page A-61, for instance, and note that these instructions require two source operands, which have to be fetched.

c) treating the first and second source operands as a set of N_1 fields. See page A-61 again and note that each source operand is divided into N_1 fields (in this case, $N_1 = 4$).

d) intermingling selected ones of the N_1 fields from the first operand and selected ones of the N_1 fields from the second operand in a second selected order in accordance with the second type of

byte intermingling instruction to form a second type of intermingled fields. See page A-61 again and note that this type of byte intermingling instruction results in selecting ones of the N_1 fields from both the first and second source operands.

e) writing a destination operand with the second type of intermingled fields. See page A-61 and note that the intermingled fields are written to a destination operand (in this case, register rdest).

47. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Intel in view of Hennessy, as applied above, in view of Haataja, U.S. Patent No. 6,137,836.

48. Referring to claim 11, Intel in view of Hennessy has taught a digital system as described in claim 1. Intel in view of Hennessy has not taught that the digital system is a cellular telephone comprising the components set forth in claim 11. However, Haataja has taught a cellular telephone comprising:

a) an integrated keyboard connected to the CPU via a keyboard adapter. See Fig.8, component 72.

b) a display, connected to the CPU via a display adapter. See Fig.8, component 36.

c) radio frequency (RF) circuitry connected to the CPU. See Fig.8, component 56, and column 7, lines 6-11.

d) an aerial connected to the RF circuitry. See Fig.8, component 54.

It should be realized that Intel in view of Hennessy has taught a system that includes operations that increase the functionality of the system. A person of ordinary skill in the art would have recognized that an improved processor (with more functionality) would lead to the overall improvement of the device in which it is embedded. As shown in Fig.8 of Haataja, and, as is

well known in the art, cellular telephones are controlled by some sort of processor. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the incorporate the digital system of Intel in view of Hennessy into a cell phone, as taught by Haataja, in order to improve the overall performance of the cell phone.

49. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Philips in view of Hennessy, as applied above, in view of Haataja, as applied above.

50. Referring to claim 11, Philips in view of Hennessy has taught a digital system as described in claim 1. Philips in view of Hennessy has not taught that the digital system is a cellular telephone comprising the components set forth in claim 11. However, Haataja has taught a cellular telephone comprising:

a) an integrated keyboard connected to the CPU via a keyboard adapter. See Fig.8, component 72.

b) a display, connected to the CPU via a display adapter. See Fig.8, component 36.

c) radio frequency (RF) circuitry connected to the CPU. See Fig.8, component 56, and column 7, lines 6-11.

d) an aerial connected to the RF circuitry. See Fig.8, component 54.

It should be realized that Philips in view of Hennessy has taught a system that includes operations that increase the functionality of the system. A person of ordinary skill in the art would have recognized that an improved processor (with more functionality) would lead to the overall improvement of the device in which it is embedded. As shown in Fig.8 of Haataja, and, as is well known in the art, cellular telephones are controlled by some sort of processor. And, as

disclosed by Philips on page 2-1, the digital system (TM1000) is used in high-quality video and audio applications (including other types of phones, such as video phone). Therefore, in order to allow cellular telephones to achieve a high level of audio quality, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the incorporate the digital system of Philips in view of Hennessy into a cell phone, as taught by Haataja, in order to improve the overall performance of the cell phone.

Conclusion

51. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

Abdallah et al., U.S. Patent No. 6,115,812, has taught a method and apparatus for efficient vertical SIMD computations. In addition, multiple unpack and shuffle operations have been disclosed.

Dulong et al., U.S. Patent No. 5,757,432, has taught manipulating video and audio signals using a processor which supports SIMD instructions. In addition, different types of unpack and shift operations have been disclosed.

Sidwell et al., U.S. Patent No. 5,875,355, has taught a method for transposing a multi-bit

matrix wherein first and last substrings remains unchanged while intermediate substrings are interchanged. This patent shows multiple operands involved in different types of byte intermingling operations.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David J. Huisman whose telephone number is (703) 305-7811. The examiner can normally be reached on Monday-Friday (8:00-4:30).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

DJH
David J. Huisman
September 11, 2003

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